Extending Atmel IDS flow

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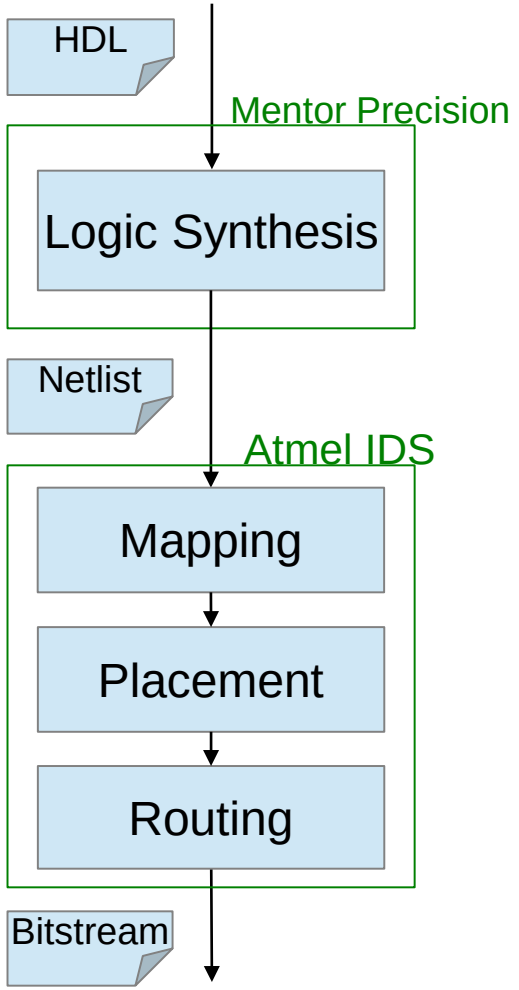
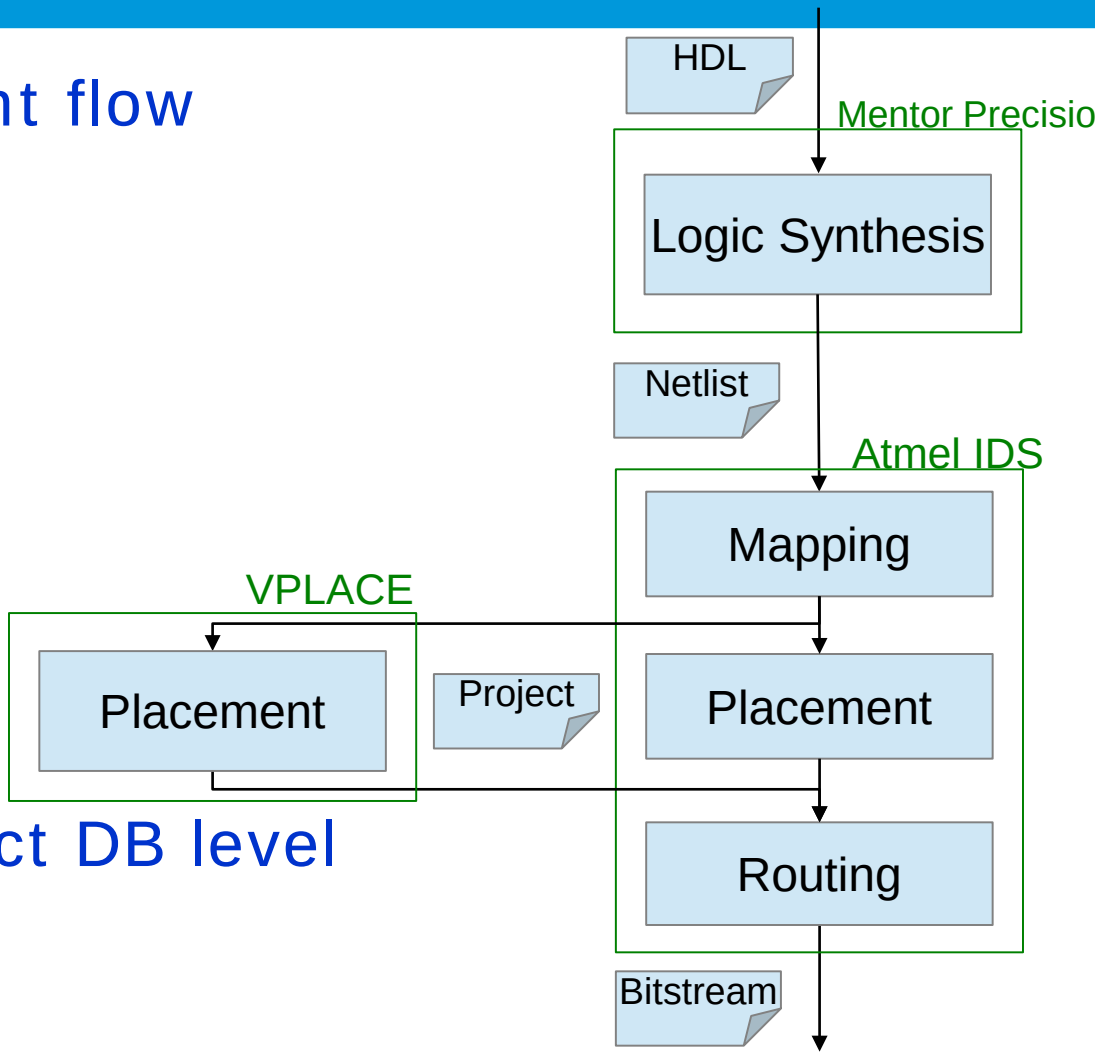
Default Precision/IDS Flow

- Implementation for Atmel FPGAs
- Starting with HDL (Verilog/VHDL) specification
- Logic Synthesis with Mentor Precision
- FPGA implementation with Atmel IDS
- But, Atmel IDS received no significant updates recently
  - Usability issues
  - No state of the art algorithms



Proposed Flow

- Automate the development flow
  - Use of Makefiles
  - Constraint generation
  - Tools invocation
- Replace IDS placement
  - Work in the IDS project DB level
  - Use VPLACE algorithm
  - Compare the two results



VPLACE

- Academic placement algorithm for FPGAs
  - Developed in Politecnico di Torino, Italy
  - Already used for Xilinx FPGAs
- Not optimized for our project yet
  - Not timing-driven
  - Not tuned for Atmel architecture
  - But, already promising results

Methodology

- Compare the two flows
  - Implementation targeting ATF280
  - IDS vs VPLACE placement
  - Resulting performance (circuit period)
- Use designs of interest
  - ITC benchmarks (for initial verification)
  - HurriCANe (CAN bus)
  - Space Wire in progress

Results

- Preliminary
  - VPLACE is still not optimized
    - Suboptimal results
    - Route congestion for some circuits
  - No exploration of critical paths yet
- Promising
  - 14% average period overhead on 21 ITC designs
    - Up to 13% improvement in some cases
  - 15% period improvement on HurriCANe 5.2.4

Conclusions

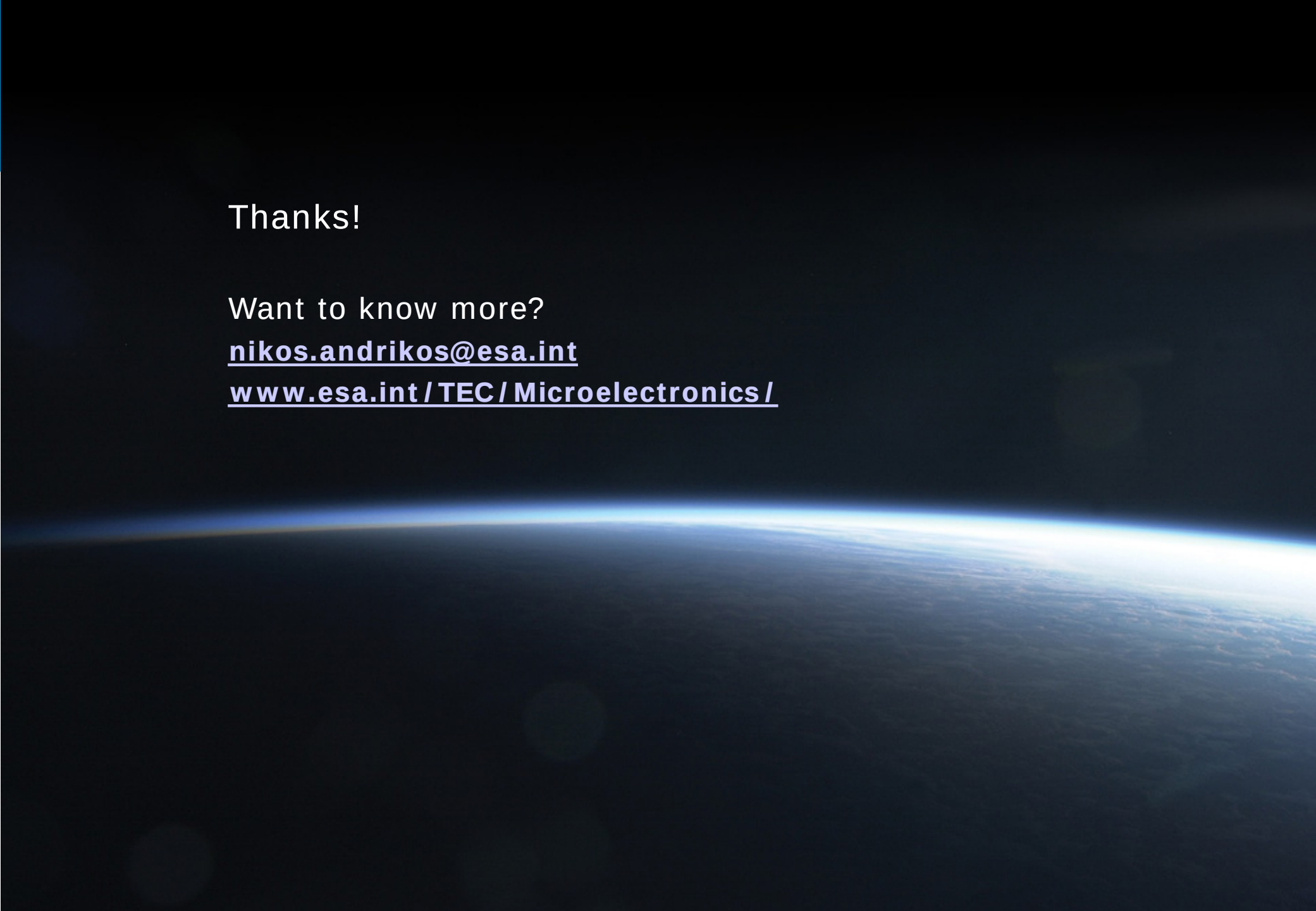
- Fully Automated Atmel IDS flow
  - More user friendly
  - Unattended runs
  - Fast constrain exploration
- VPLACE placement algorithm
  - Integrates with Atmel IDS
  - Alternative to IDS default placement
  - Not fully tuned yet
    - But, promising results already

Results – Timing

Design	Figaro	VPlace	Diff %	Design	Figaro	VPlace	Diff %
HurriCANe	108.1	91.7	-15.2	b13	25.1	29.5	17.7
b01	9.8	17.0	72.6	b14	164.8	174.3	5.7
b02	8.6	11.4	31.7	b14_1	174.8	166.8	-4.6
b03	25.6	38.4	50.0	b15	131.4	126.5	-3.7
b04	42.4	-	N/A	b15_1	123.9	124.7	0.7
b05	47.9	49.4	3.0	b17	202.2	-	N/A
b06	9.2	16.0	74.3	b17_1	-	233.4	N/A
b07	32.3	31.9	-1.4	b20	203.3	184.6	-9.2
b08	34.6	46.4	33.9	b20_1	190.7	165.4	-13.3
b09	25.7	-	N/A	b21	184.7	178.5	-3.4
b10	23.8	37.0	55.3	b21_1	170.5	165.4	-3.0
b11	39.2	36.1	-7.9	b22	174.1	166.0	-4.6
b12	59.1	56.3	-4.8	b22_1	173.4	182.0	5.0

Period (ns)

Period (ns)



Thanks!

Want to know more?

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